

THE CLAIMS

What is claimed is:

1. A processor including:

a first register for storing a first packed data;

a decoder having a control signal input, said control signal input for receiving a first control signal, and a second control signal, said first control signal for indicating a pack operation, said second control signal for indicating an unpack operation;

a functional unit being coupled to said decoder and said first register, said functional unit for performing said pack operation and said unpack operation using said first packed data.

2. The processor of claim 1 wherein said first packed data includes a plurality of data elements, each data element of said plurality of data elements has a size, and said first control signal further includes an indicator corresponding to said size.

3. The processor of claim 2 wherein said size is one of packed byte, packed word, and packed doubleword.

4. The processor of claim 2 where said first packed data is sixty-four bits.

5. The processor of claim 1 wherein said first control signal includes a source address.

6. The processor of claim 1 wherein said first control signal includes a sign indicator, said sign indicator for determining whether said pack operation is to be performed signed or unsigned.

7. The processor of claim 1 wherein said control signal input is further for receiving a third control signal, said third control signal for indicating a move operation, wherein said processor further includes a second register, said second register for storing integer data, and wherein said move operation causes said processor to move data between said first register and said second register.

8. The processor of claim 1 wherein said processor includes a register file, said register file includes a register, and wherein said first control signal and said second control signal include a second location and said second location corresponds to said register, wherein said functional unit is further for generating a result from an execution of an operation, and wherein said result is stored at said second location.

9. The processor of claim 1 wherein said processor first control signal includes a second location and said second location corresponds to a memory location, wherein said functional unit is further for generating a result from an execution of an operation, and wherein said result is stored at said second location.

10. A method of manipulating packed data in a processor, said processor having a decoder, a functional unit, a first register and a second register, said decoder being coupled to said functional unit, said first register and said second register, said method comprising the steps of:

said decoder decoding a control signal;

if said decoder determines that said control signal indicates a pack operation,

then said processor performing the following steps,

accessing a first packed data stored in said first register,

accessing a second packed data stored in said second register,

packing said first packed data with said second packed data to

generate a result packed data,

storing said result packed data in said first register;

if said decoder determines that said control signal indicates an unpack

operation, then said processor performing the following steps,

accessing said first packed data stored in said first register,

accessing said second packed data stored in said second register,

unpacking said first packed data and said second packed data to

generate said result packed data,

storing said result packed data in said first register; and

if said decoder determines that said control signal indicates a move

operation, then said processor performing the following steps,

accessing said second packed data stored in said second register,
storing a portion of said second packed data in a third register, said
third register for storing integer data.

11. The method of claim 10 wherein said packing is performed without
saturation and wherein said packing includes accessing the low order bits of each
data element in said first packed data and said second packed data, and wherein said
low order bits are included in said result packed data.

12. The method of claim 10 wherein said first packed data includes a first
plurality of data elements, each data element of said first plurality of data elements
being represented by a first predetermined number of bits, said control signal
includes a size indicator, said size indicator indicating said first predetermined
number of bits, and wherein said result packed data includes a second plurality of
data elements, said second plurality of data elements having twice as many data
elements as said first plurality of data elements, and each data element of said
second plurality of data elements being represented by a second predetermined
number, and said second predetermined number of bits being half as much as said
first predetermined number of bits.

13. The method of claim 10 wherein said first packed data includes a first set of
data elements, and wherein said second packed data includes a second set of data
elements, and wherein said unpacking includes interleaving low order data elements

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